a module solution provider

WG7310-00 WLAN+BT+FM Module

TI WL1271 solution

Hardware Design Guide

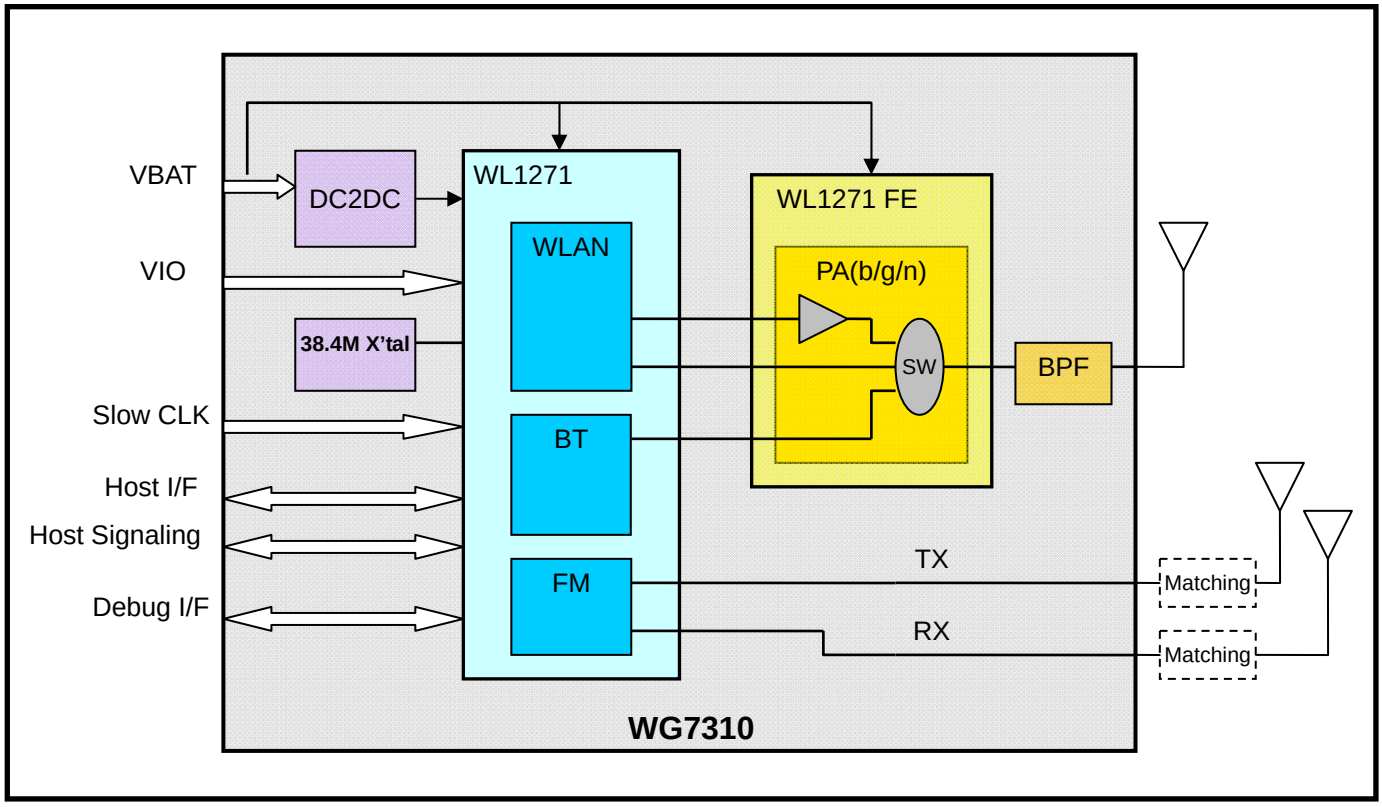
Revision 0.3

Contents

1. WG7310 Module Description

WG7310, a WLAN , Bluetooth and FM SiP (system in package) module, is the most demanded design for all handset and portable devices with TI WL1271 IEEE 802.11b/g/n and BT v2.1 EDR solutions to provide the best WLAN and BT coexistence interoperability and power saving technologies from TI.

1.1. WG7310 Block Diagram



1.2. Pin Description

No.	Index	Name	Type	Description
1	A1	GND	GND	GROUND
2	A2	VBAT_FEM	O	FEM POWER SUPPLY
3	B1	BT_FUNC2: BT_WU/ DC2DC	O	BT WU (default) or BT DC2DC
4	B2	GND	GND	GROUND
5	C1	BT_FUNC6: BT_SDA	O	BT SDA (internal use only)
6	C2	BT_FUNC4: BT_TX_DBG	O	BT UARTD (reserved for debug)
7	D1	BT_FUNC5: HOST_WU	O	HOST WU
8	D2	GND	GND	GROUND
9	E1	GND	GND	GROUND
10	E2	DRPWPABC	O	WL PA BIAS (internal use only)
11	F1	BT_RF_ANT	I/O	BT RF ANT (internal use only)
12	F2	GND	GND	GROUND
13	G1	GND	GND	GROUND
14	G2	DRPWPDET	I	WL POWER DET IN (internal use only)
15	H1	WL_TX_SW	O	WLPA_IF (internal use only)
16	H2	GND	GND	GROUND
17	J1	WL_BTH_SW	O	WLPA_IF (internal use only)
18	J2	WL_RX_SW	O	WLPA_IF (internal use only)
19	K1	GND	GND	GROUND
20	K2	VCC_DCOW	O	WL DCO SUPPLY
21	L1	NC_C3/VCC_TXAW	O	WL PPA A SUPPLY
22	L2	GND	GND	GROUND
23	L3	FM_EN	I	FM RST
24	K3	VCC_RXW	O	WL LNA SUPPLY
25	L4	GND	GND	GROUND
26	K4	BT_EN	I	BT RST
27	L5	WB_RF_ANT	I/O	WL/BT RF ANT
28	K5	GND	GND	GROUND
29	L6	GND	GND	GROUND
30	K6	WL_RS232_RX/ I2S_M_SCL	I	RS232_RX (default) or I2C_M_SCL (reserved for debug)
31	L7	SDIO_D1	I/O	SDIO IF
32	K7	WL_RS232_TX/ I2S_M_SDA	O	RS232_TX (default) or I2C_M_SDA

				(reserved for debug)
33	L8	SDIO_D2	I/O	SDIO IF
34	K8	SPI_CSX/ SDIO_D3	I/O	SDIO IF
35	L9	SPI_DIN/ SDIO_CMD	I/O	SDIO IF
36	K9	SPI_DOUT/ SDIO_D0	I/O	SDIO IF
37	L10	SPI_CLK/ SDIO_CLK	I	SDIO IF
38	K10	FM_I2S_FSYNC	I/O	FM I2S IF
39	L11	WL_EN	I	WL RST
40	K11	FM_SDA	I/O	FM I2C IF
41	J11	FM_SCL	I/O	FM I2C IF
42	J10	FM_IRQ	O	FM I2C IF
43	H11	FM_I2S_CLK	I/O	FM I2S IF
44	H10	FM_I2S_DI	I	FM I2S IF
45	G11	FM_I2S_DO	O	FM I2S IF
46	G10	GND	GND	GROUND
47	F11	GND	GND	GROUND
48	F10	SLOWCLK	I	SLEEP CLK
49	E11	FM_TX_ANT	O	FM TX ANT
50	E10	GND	GND	GROUND
51	D11	GND	GND	GROUND
52	D10	FMAUDROUT	O	FM AUD OUT
53	C11	FM_RX_ANT	I	FM RX ANT
54	C10	GND	GND	GROUND
55	B11	GND	GND	GROUND
56	B10	FMAUDLOUT	O	FM AUD OUT
57	A11	FMAUDRIN	I	FM AUD IN
58	A10	GND	GND	GROUND
59	A9	FMAUDLIN	I	FM AUD IN
60	B9	GND	GND	GROUND
61	A8	GND	GND	GROUND
62	B8	XTALP	O	FREF INPUT (internal use only)
63	A7	XTALM	O	FREF INPUT (internal use only)
64	B7	GND	GND	GROUND
65	A6	GND	GND	GROUND
66	B6	BT_FUNC1:	O	BT DC2DC mode (default)

		DC2DC/ btSPI_CLK		or btSPI_CLK
67	A5	DC_REQ	O	DC_REQ to INTERNAL DC2DC
68	B5	TPS_DC2DC	I	MODE SELECTION PIN OF DC2DC
69	A4	VIO	I	1.62~1.92V POWER SUPPLY, 1.8V TYP
70	B4	1V8	O	1.8V DC2DC POWER SUPPLY
71	A3	VBAT	I	2.3~4.8V POWER SUPPLY, 3.3V TYP
72	B3	VDD_LDO_IN_CLASS1P5	I	BT CLASS2/CLASS1.5 POWER SUPPLY
73	D4	PCM_AUD_CLK/ FM_I2S_CLK	I/O	PCM I/F (default) or FM I2S CLK
74	E4	PCM_AUD_IN/ FM_I2S_DI	I/O	PCM I/F (default) or FM I2S DI
75	F4	GND	GND	GROUND
76	G4	WL_PAEN_B	O	WLPA_IF (internal use only)
77	H4	GND	GND	GROUND
78	H5	VCC_ANAW	O	WLANA INPUT SUPPLY
79	H6	VCC_TXBW	O	WL PPA BG SUPPLY
80	H7	WL_UART_DBG	O	WL_UART_DBG (reserved for debug)
81	H8	CLK_REQ_OUT	O	CLK_REQ positive polarity
82	G8	WLAN_IRQ	O	WLAN interrupt request
83	F8	HCI_RX/ btSPI_DIN	I	BT UART I/F (default) or btSPI DIN
84	E8	HCI_TX/ btSPI_DOUT	O	BT UART I/F (default) or btSPI DOUT
85	D8	BT_FUNC7: BT_SCL	I/O	BT_SCL (internal use only)
86	D7	HCI_RTS/ btSPI_IRQ	I/O	BT UART I/F (default) or btSPI IRQ
87	D6	HCI_CTS/ btSPI_CS	I/O	BT UART I/F (default) or btSPI CS
88	D5	PCM_AUD_FSYNC/ FM_I2S_FSYNC	I/O	PCM I/F (default) or FM I2S FSYNC
89	E5	PCM_AUD_OUT/ FM_I2S_DO	O	PCM I/F (default) or FM_I2S_DO
90	F5	GND	GND	GROUND
91	G5	GND	GND	GROUND
92	G6	GND	GND	GROUND
93	G7	GND	GND	GROUND
94	F7	GND	GND	GROUND
95	E7	GND	GND	GROUND
96	E6	GND	GND	GROUND

2. Electrical Characteristics

2.1. Absolute Maximum Ratings

Over operating free-air temperature range

Characteristics		Value	Unit
Supply Voltage Range	VBAT	-0.5 to 5.5	V
	VIO	-0.5 to 2.1	V
Input Voltage to Analog Pins		-0.5 to 2.1	V
Input Voltage to all Other Pins		-0.5 to VIO + 0.5V	V
Operating Ambient Temperature Range		-20 to 70	˚C
Storage Temperature Range		-45 to 85	˚C

2.2. Recommended Operating Conditions

The WG7310 requires two supplies: VBAT and VIO.

Power Supply	Voltage		
	Min.	Typ.	Max.
VBAT	2.7V	3.3V	4.8V
VIO	1.62V	1.8V	1.92V

2.3. External Slow Clock Input (SLEEP_CLK)

The external slow clock input SLEEP_CLK must be present at all times. The slow clock is used to maintain timers that synchronize the device to the access point (AP) beacons.

Table 1. External Slow Clock Input Requirements

Characteristics	Condition	Min.	Typ.	Max.	Unit
Frequency			32.768		KHz
Reference Frequency Accuracy	WLAN, BT, FM_RX			+/-150	ppm
	FM_TX			+/- 40	
Input Transmit Time	10% ~ 90%			100	ns

Frequency Duty Cycle		30	50	70	%
Fail Safe Maximum Value				2.0	V
Input Voltage Limits (Square Wave)	V_{IH}	0.65xVIO		VIO	V_{peak}
	V_{IL}	0		0.35xVIO	
Input Impedance		1			MΩ
Input Capacitance				5	pF
Rise and fall time				100	ns
Phase noise	1kHz		-125		dBc/Hz

3. Power Sequence

3.1. WLAN Power on Sequence

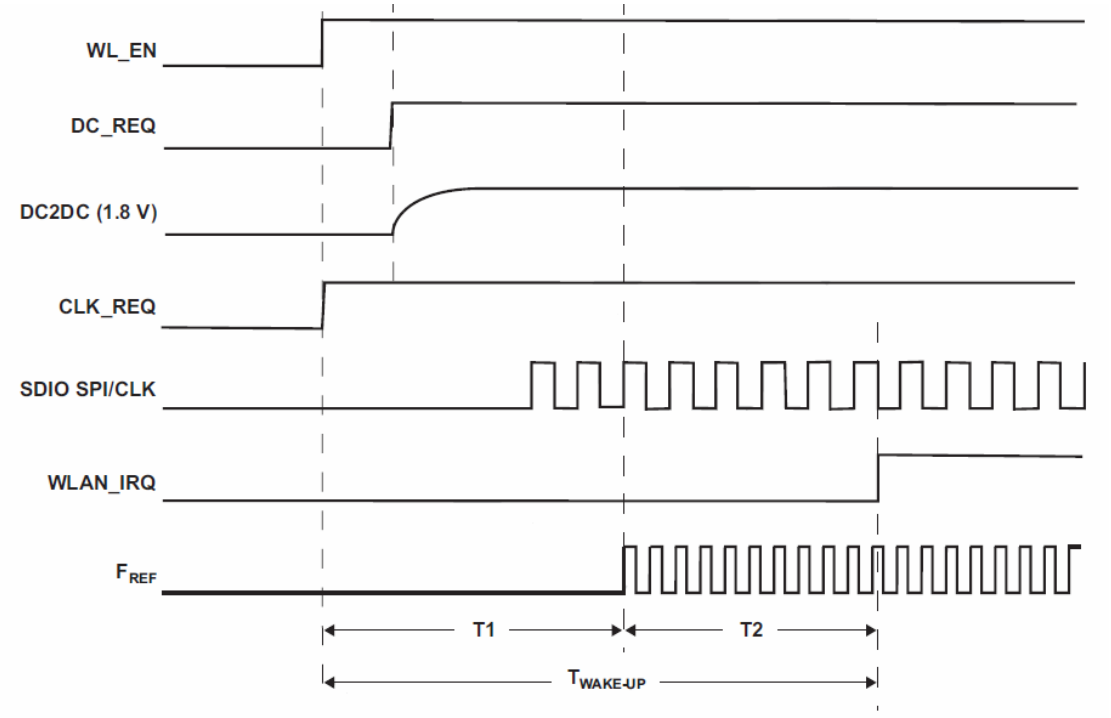


Figure 1. WLAN Power on sequence

The duration of T1 is defined as the time from WL_EN=high until Fref is valid for the SoC.

T1 ~ 55ms

The duration of T2 depends on:

- Operation system
- Host enumeration for the SDIO/SPI
- PLL configuration
- Firmware download
- Releasing the core from reset
- Firmware initialization

3.2. Bluetooth Power Up/Down Sequence

Power up requirements:

1. BT_EN must be low
2. VIO must be stable before releasing BT_EN.
3. Slow clock must be stable within 2 ms of BT_EN high.

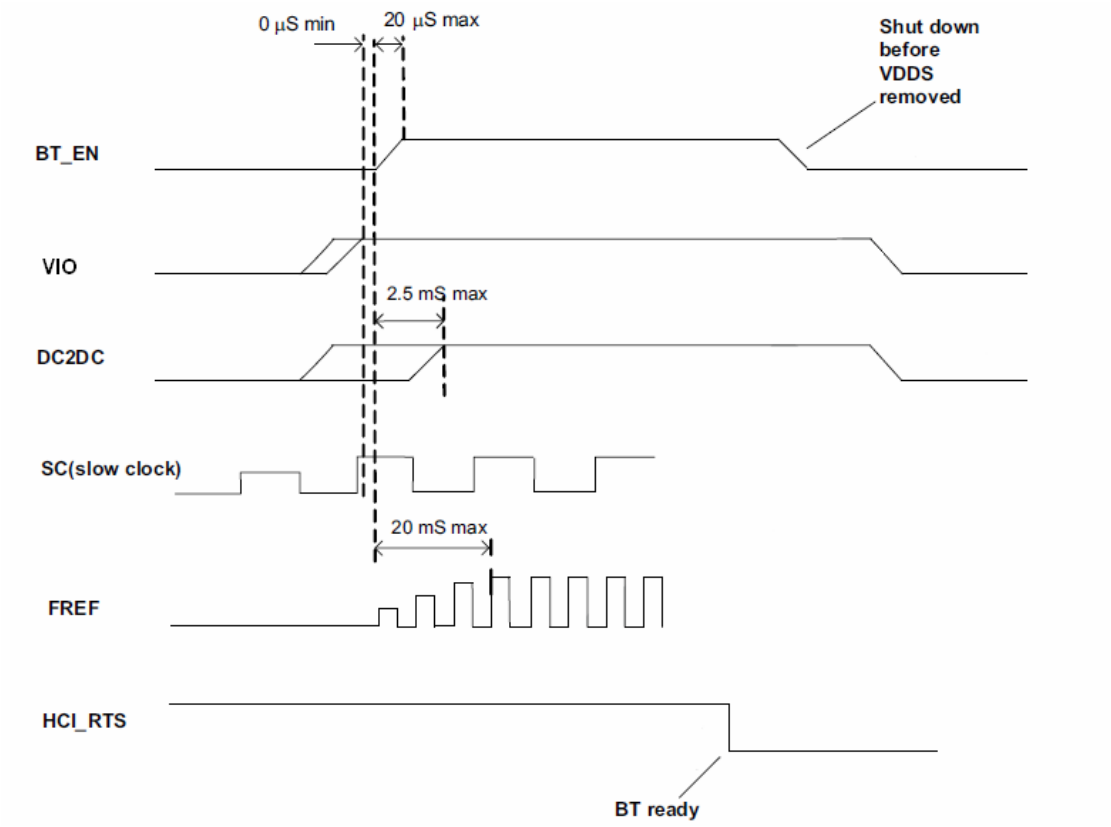


Figure 2. Bluetooth Power Up/Down sequence

WG7310 indicates completion of power up sequence by asserting RTS low. This occurs up to 100ms after BT_EN goes high.

4. Interface Characteristics

4.1. WLAN SDIO Characteristic

4.1.1. SDIO Read Timing

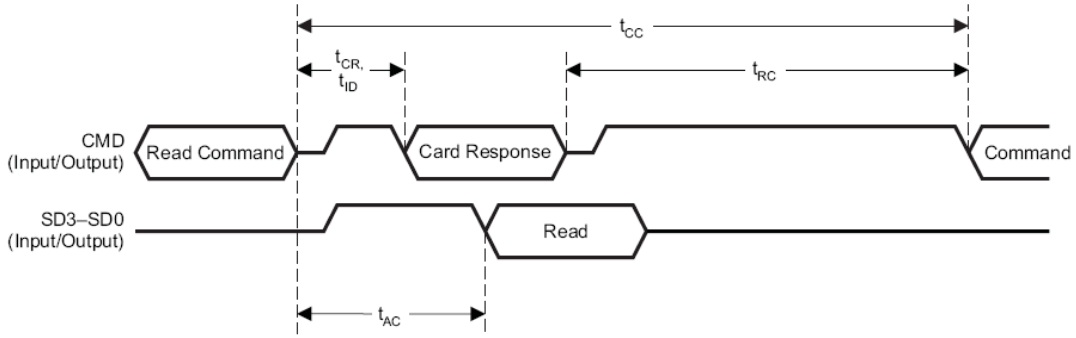
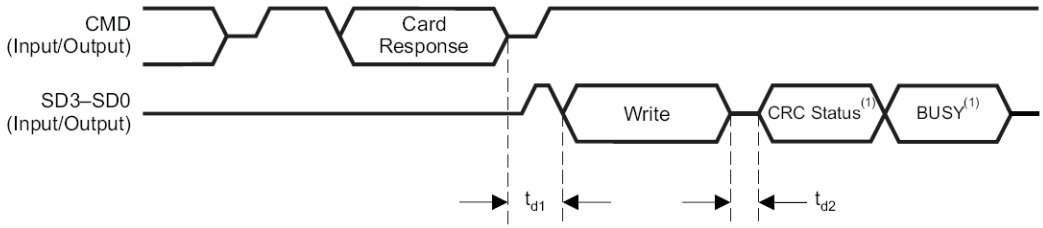


Figure 3. SDIO Single Block Read

Table 2. SDIO Read Switching characteristics

Parameter		Min.	Max.	Unit
t_{CR}	Delay time, assign relative address/data transfer mode, CMD command invalid to CMD response valid	2	64	Clock Cycles
t_{ID}	Delay time, identification, CMD command invalid to CMD response valid	5	5	
t_{CC}	Delay time, CMD command invalid to CMD response valid	8	---	Clock Cycles
t_{RC}	Delay time, CMD response invalid to CMD command valid	8	---	Clock Cycles
t_{AC}	Access time, CMD command invalid to SD3-SD3 read data valid	2	---	Clock Cycles

4.1.2. SDIO Interface Write Timing



(1) CRC status and busy waveforms are only for data line 0. Data lines 1-3 are N/A. The busy waveform is optional and may not be present.

Figure 4. SDIO Single Block Write

Table 3. SDIO Write Switching characteristics

Parameter		Min.	Max.	Unit
t_{d1}	Delay time, CMD card response invalid to SD3-SD0 write data valid	2	---	Clock Cycles
t_{d2}	Delay time, SD3-SD0 write data invalid end to CRC status valid	2	2	Clock Cycles

4.1.3. SDIO Clock Timing

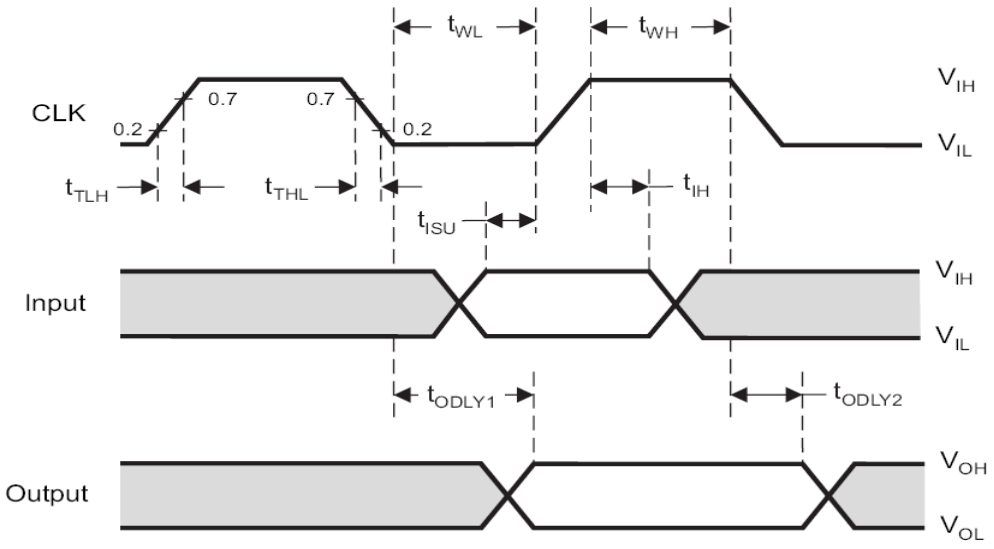


Figure 5. SDIO Clock Timing

Table 4. SDIO Timing requirement

Parameter		Min.	Max.	Unit
f_{clock}	Clock frequency, CLK	0	25	MHZ
DC	Low/high duty cycle	40	60	%
t_{WL}	Pulse duration, CLK low	10		ns
t_{WH}	Pulse duration, CLK high	10		ns
t_{TLH}	Rise time, CLK		4.3	ns
t_{THL}	Fall time, CLK		3.5	ns
t_{ISU}	Setup time, input valid before CLK↑	5		ns
t_{1H}	Hold time, input valid after CLK↑	5		ns
t_{ODLY1}	Delay time, CLK↓ to output valid	0	14	ns
T_{ODLY2}	Delay time, CLK↓ to output invalid	0	14	ns

4.2. WLAN wSPI Characteristics

The SPI interface signals are shared with the SDIO bus in the WG7310.

4.2.1. SPI Read/Write Timing

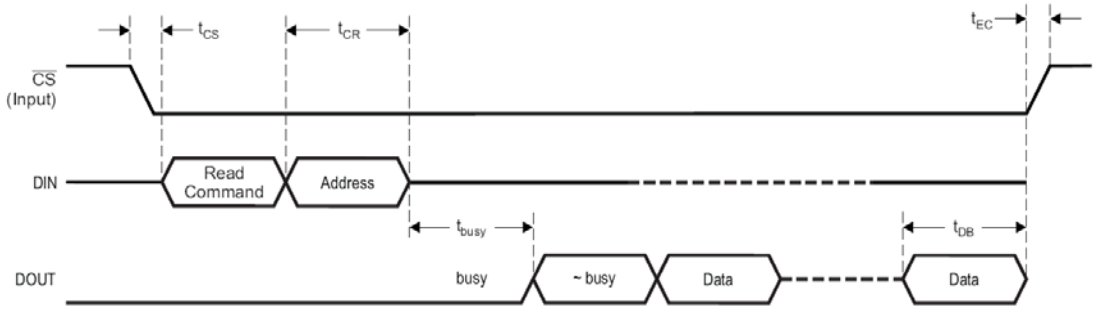


Figure 6. SPI Read Timing

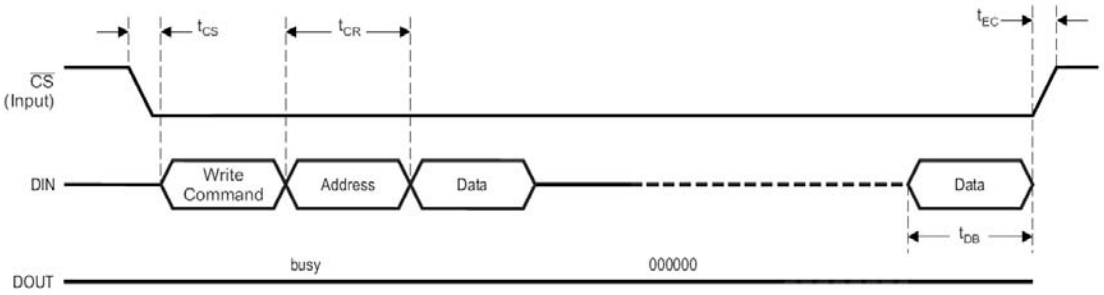


Figure 7. SPI Write Timing

Table 5. SPI Read/Write Switching characteristics

Parameter		Min.	Max.	Unit
t_{CS}	Delay time, CS ↓ to DIN read/write command valid	0		16 Clock Cycles
t_{CR}	Delay time, DIN read command invalid to DOUT/DIN card response valid		1	16 Clock Cycles
t_{busy}	Fixed busy delay till DOUT data valid	1	7	16/32 Clock Cycles
t_{EC}	Delay time, DOUT data invalid CS ↑	0		16 Clock Cycles
t_{DB}	Data block size		1	16/32 Clock Cycles

4.2.2. SPI Clock Timing

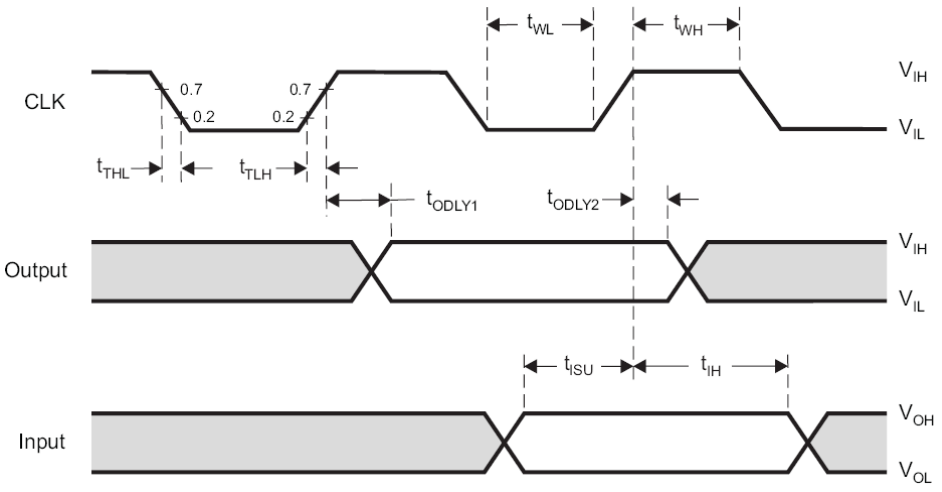
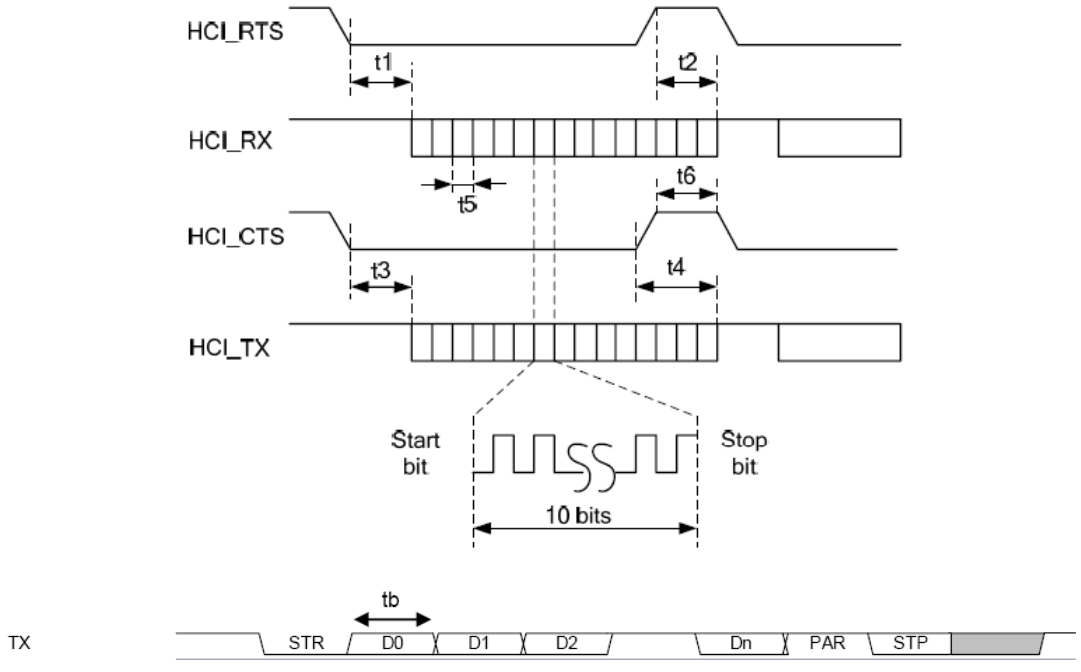


Figure 8. SPI Clock Timing

Table 6. SPI Timing requirement

Parameter		Min.	Max.	Unit
f_{clock}	Clock frequency, CLK	0	48	MHZ
DC	Low/high duty cycle	40	60	%
t_{WL}	Pulse duration, CLK low	5		ns
t_{WH}	Pulse duration, CLK high	5		ns
t_{TLH}	Rise time, CLK		4.3	ns
t_{THL}	Fall time, CLK		3.5	ns
t_{ISU}	Setup time, input valid before CLK↑	5		ns
t_{1H}	Hold time, input valid after CLK↑	5		ns
t_{ODLY1}	Delay time, CLK ↑ to output valid	4	15	ns
T_{ODLY2}	Delay time, CLK ↓ to output invalid	5	15	ns

4.3. Bluetooth HCI Interface



* STR: Start bit; D0…Dn: Data bits (LSB first); PAR: Parity bit (if parity is used); STP: Stop bit

Table 7. BT HCI Timing characteristics

Characteristics	Condition	Symbol	Min	Typ.	Max	Unit
Baud rate	Any rate (1)		37.5	115.2	4000	kbps
Baud rate accuracy	Receive/Transmit	t5/t7			-2.5to+1.5	%
CTS low to TX_DATA on		t3	0	2		us
CTS high to TX_DATA off	Hardware flow control	t4			1	Byte
CTS high pulse width		t6	1			bit
RTS low to RX_DATA on		t1	0	2		us
RTS high to RX_DATA off	Interrupt set to 1/4 FIFO	t2			16	Bytes

(1) Exception for 19.2MHz: Maximum baud rate = 3.84Mbps.

4.4. Bluetooth PCM Interface

Bluetooth can be setting as master or slave mode. For more stable voice performance, slave mode is recommended.

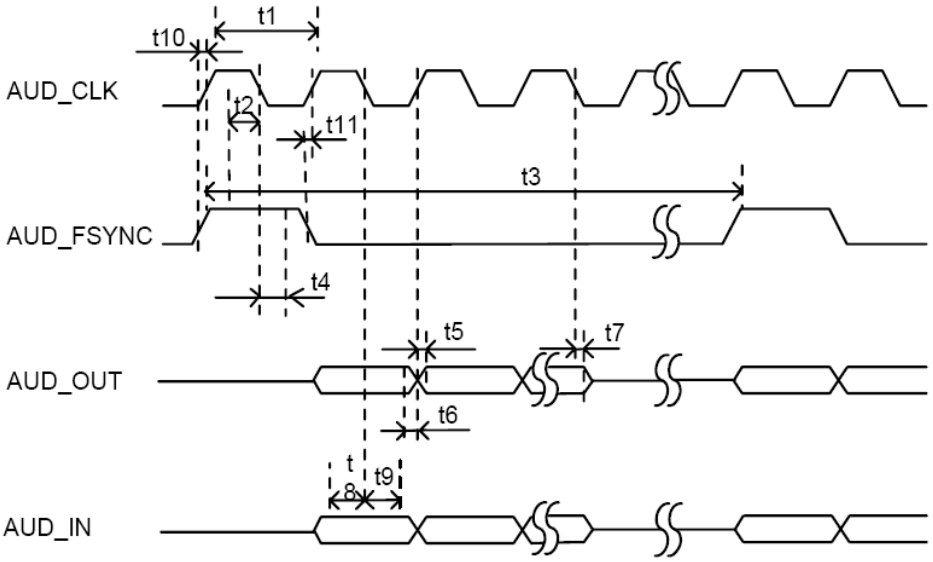


Table 8. BT PCM Slave mode Timing characteristics

Characteristics	Symbol	Min	Typ.	Max	Unit
Master clock frequency	1/t1	64		16000	KHz
Clock duty cycle		40	50	60	%

Synchronization clock frequency	1/t3	1/(8xt1)		1/(65535xt1)	KHz
Synchronization signal width		t1		165545xt1	
Setup time for AUD_FSYNC high to AUD_CLK low	t2	5			ns
Hold time from AUD_CLK low to AUD_FSYNC low	t4	8			ns
Setup time for AUD_IN valid to AUD_CLK low	t8	5			ns
Hold time from AUD_CLK low to AUD_IN invalid	t9	8			ns
Delay time from AUD_CLK high to AUD_OUT data valid	t5			20	ns
Delay time from AUD_CLK low to last data bit of AUD_OUT output set to high impedance	t7			20	ns

5. Debug Interface

The debug interface helps customers to evaluate the HW/SW features for their application. It also helps to debug during the development stage. The WG7310 module support RS232 signals and UART signals for debug purpose. Connect RS232 and UART signals to the test points for future debug support.

5.1. WLAN RS232 Testing Port

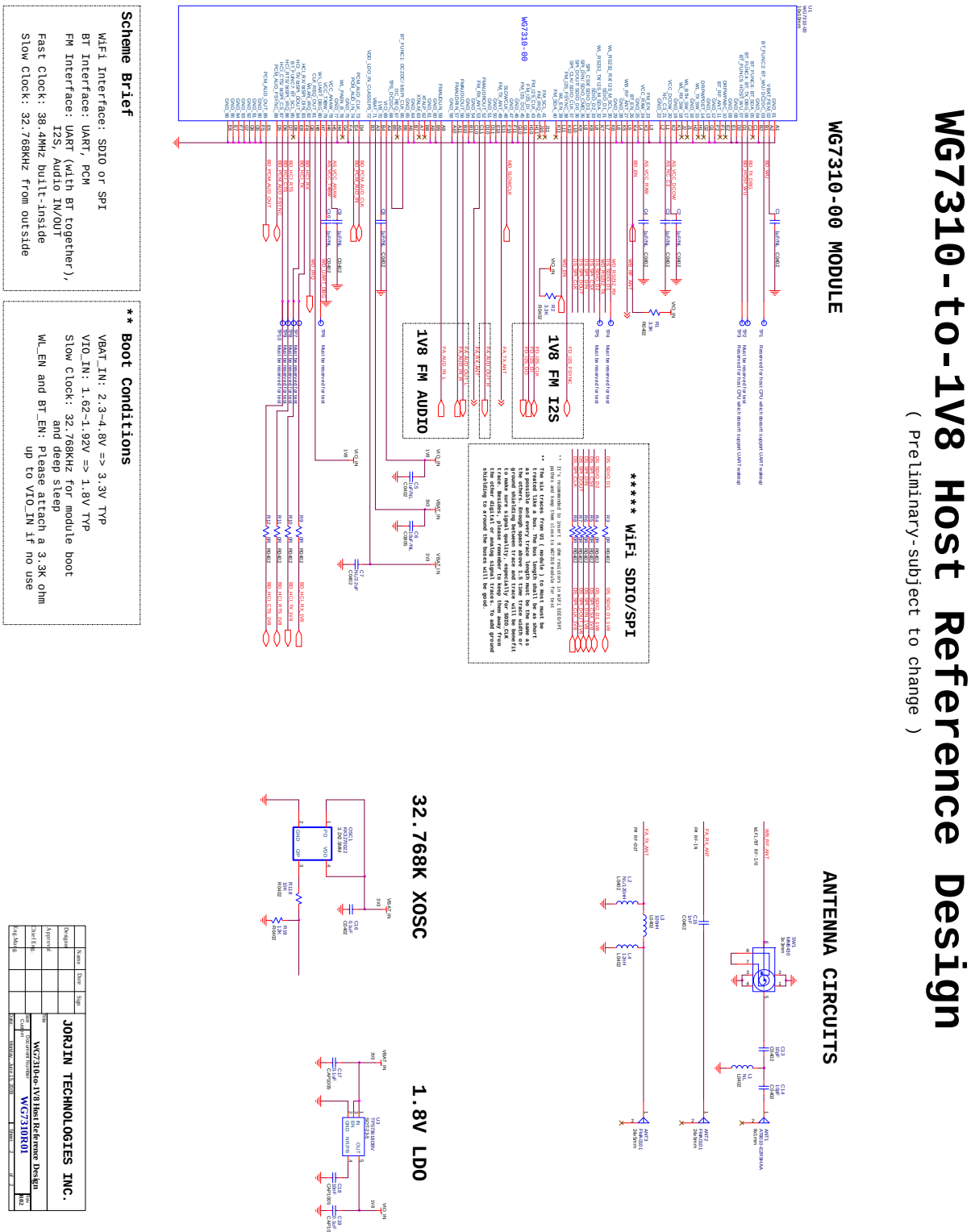
"Direct" serial interface (RS232_TX, RS232_RX) used by WLAN TrioScope software package for WLAN RF performance test, debug and manufacturing application.

5.2. Bluetooth HCI Testing Port

HCI_TX and HCI_RX are used by Bluetooth "HCI Tester" software package for Bluetooth RF performance test, debug and manufacturing application.

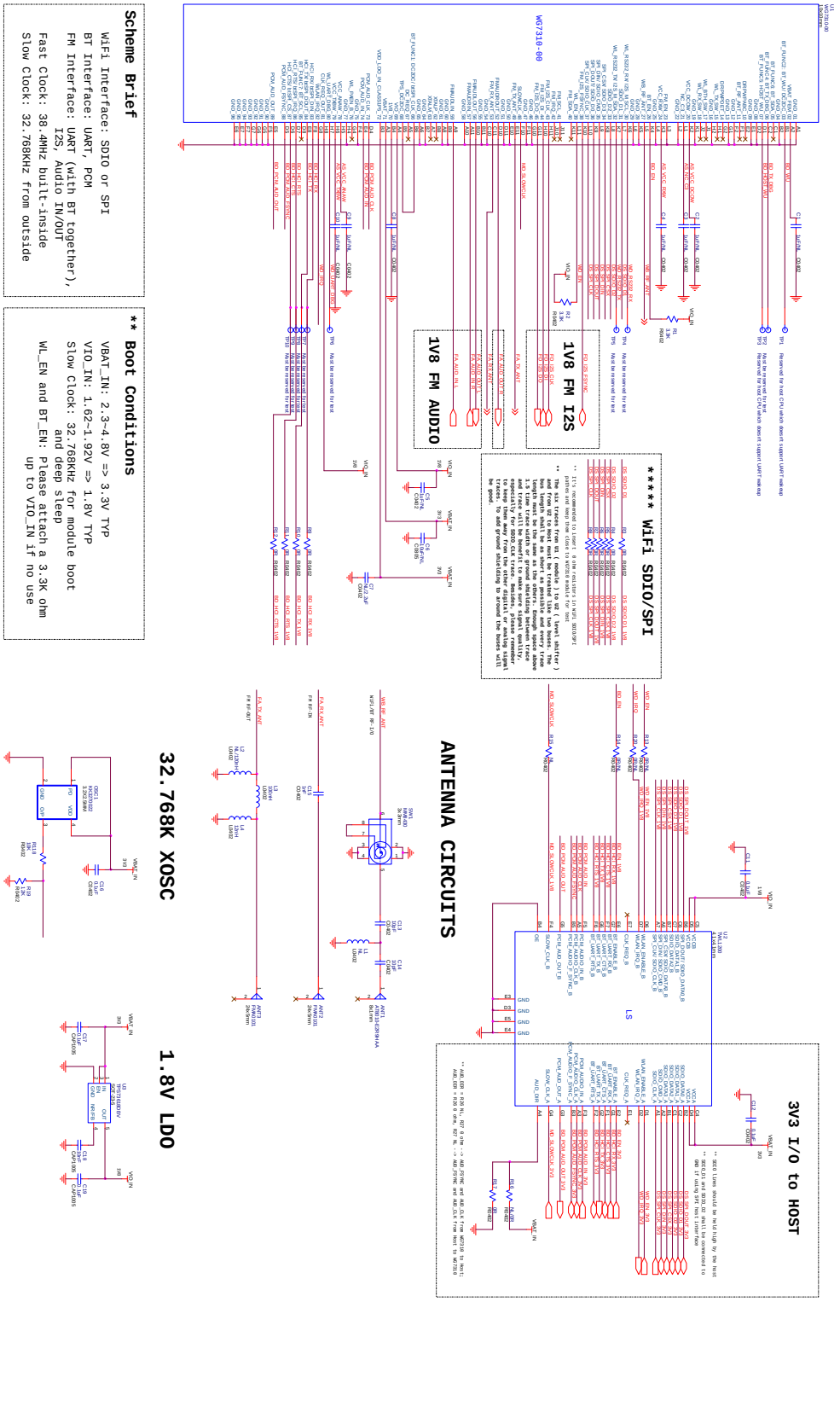
Please reserve test pads for all test ports debug purpose.

6. Reference Schematic



WG7310-to-3V3 Host Reference Design

(Preliminary-subject to change)



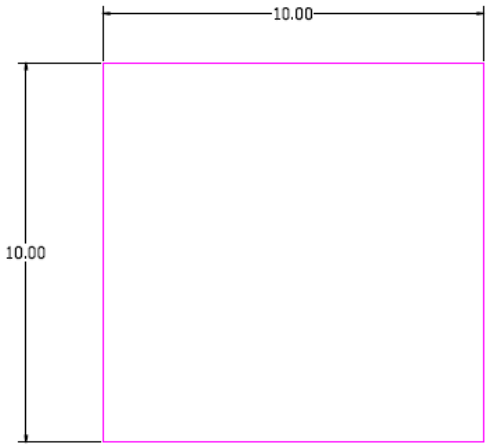
				Name	Date
Design					
Approval					
Chief Engr.					
Eng.Mgr.					

JORJIN TECHNOLOGIES INC.

Title	WG7310-to-3V3 Host Reference Design		
Size	Document Number	WG7310R00	Rev
			1.002
Date	Friday, June 19, 2009	Sheet 1	of 1

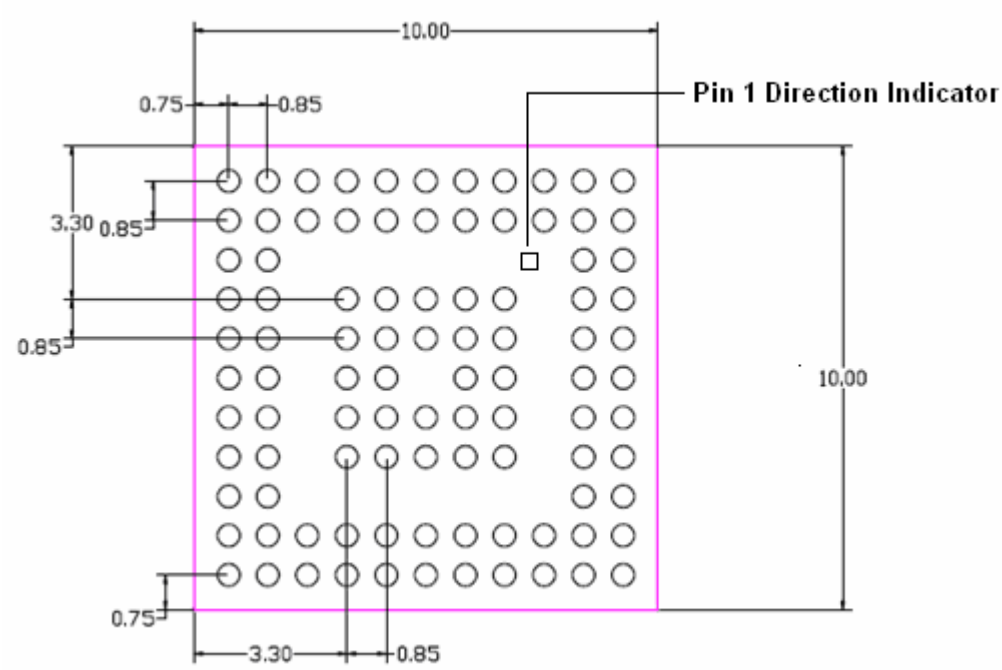
7. Module Mechanical Outline

WG7310 Bottom View



Side View

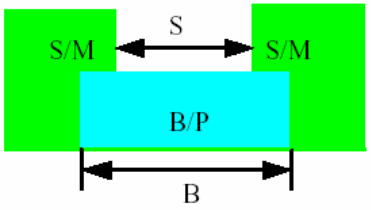
WG7310 Bottom View



- **Pin array = 11x11**
- **Pin number = 96 pins**
- **Bump pitch = 0.85mm**
- **Bump diameter = 0.5mm**

8. Layout Recommendation

8.1. Recommended Bump Pad Design *



Item	Recommend	Unit
"B" Bump pad diameter on SMD PCB	600	um
"S" Solder Mask Opening	400	um

Figure 9. Recommended Bump Pad Design

COMMENT:

SMD = Solder Mask Define

S/M= Solder Mask

B/P= Bump Pad

8.2. Recommended Stencil Design *

The bump pad size, it's solder mask opening and the relevant stencil via diameter described in **Section 8.1** and **Section 8.2** shall be followed completely otherwise the module mounting yield rate couldn't be insured. The recommended stencil via diameter is 570 um.

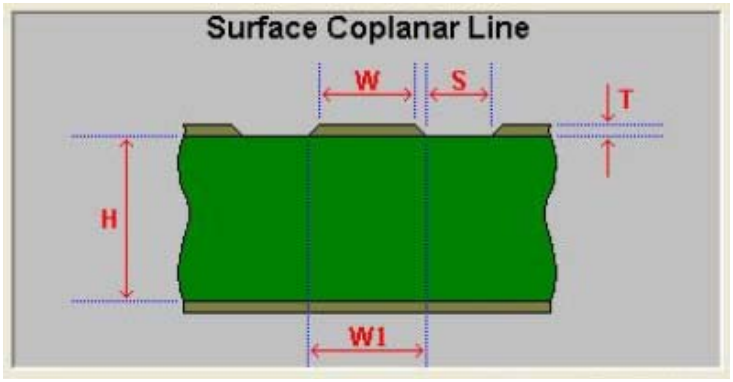
8.3. Recommended Trace Layout

- **Digital Signals Layout**
  - SDIO signals traces (CLK, CMD, D0, D1, D2 and D3) should be routed in parallel to each other and as short as possible. **Every trace length must be the same as the others.** Enough space above 1.5 time trace width or ground shielding between trace and trace will be benefit to make sure signal quality, especially for SDIO_CLK trace.

    Besides, to keep them away from the other digital or analog signal traces and to add ground plane around them are also recommended strongly.

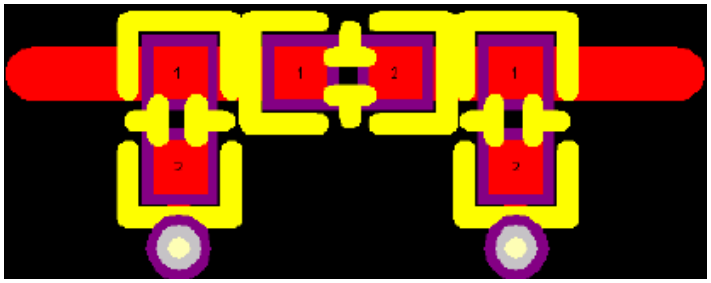
- SDIO/SPI Clock, Audio Clock (PCM_AUD_CLK), FM I2S Clock (FM_I2S_CLK), FM I2C Clock (FM_SCL), these digital clock signals are a source of noise. Keep the traces of these signals as short as possible. Whenever possible, maintain a clearance around them.

- **RF Trace & Antenna**
  - WB_RF_ANT and FM_RX_ANT are required as 50 ohm traces, and FM_TX_ANT is as 75ohm one. If 75 ohm is difficult to be achieved, FM_TX_ANT could be designed as 50 ohm also but the trace length between module to FM_TX_ANT matching circuit is recommended as short as possible.
  - Recommended 50ohm trace design for PCB layout



Height Between L1 and L2 **(H):**	10.0 mil
Trace **(W):**	14.3 mil
(W1):	14.3 mil
Thickness **(T):**	2.1 mil
Separation **(S):**	10.0 mil
Dielectric **(Er):**	4.3

  - Move all the high-speed traces and components far away from the antenna.
  - Check ANT vendor for the layout guideline and clearance.
  - Matching circuit layout should be as following figure.



- **Power Trace**
  - Power trace for VBAT should be 40mil wide. 1.8V trace should be 18mil wide.

- **Ground**
  - Having a complete Ground and more GND vias under module in layer1 for system stable and thermal dissipation as following figure.
  - Have a complete Ground pour in layer 2 for thermal dissipation.
  - Increase the GND pour in the 1st layer, move all the traces from the 1st layer to the inner layers if possible.
  - Move GND vias close to the pad.

- **Slow Clock**
  - FM RF module uses the 32-kHz clock, it is extremely important that the slow-clock trace not be routed next to any digital signals.
  - The slow clock trace should not be routed above or below digital signals on other layers.

9. SMT and Baking Recommendation

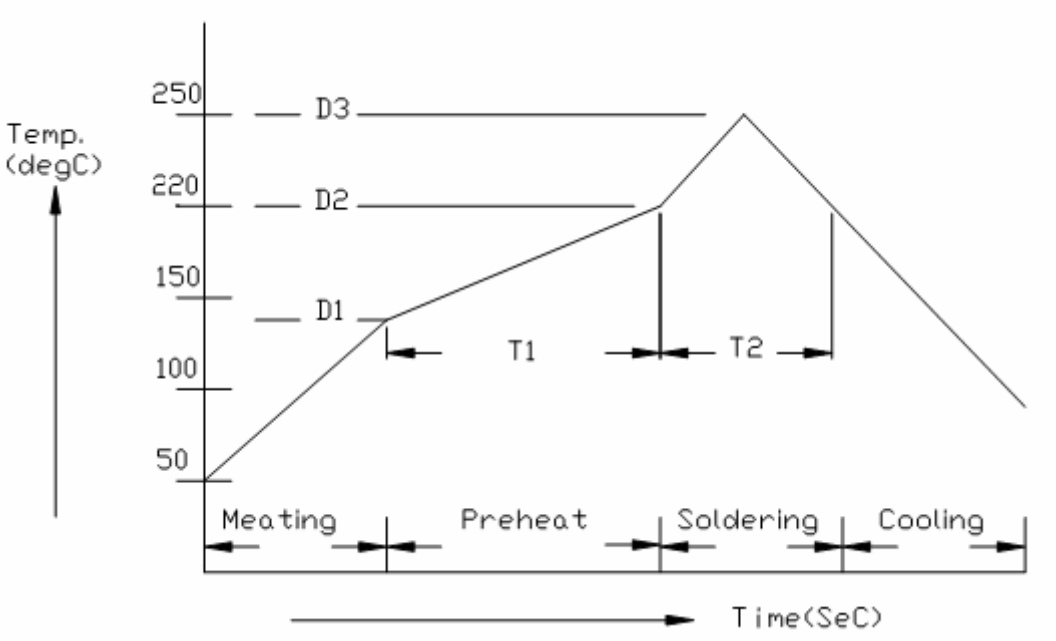
9.1. Baking Recommendation

- Baking condition：
  - Follow MSL Level 4 to do baking process.
  - After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be
    a) Mounted within 72 hours of factory conditions <30°C/60% RH, or
    b) Stored at <10% RH.
  - Devices require bake, before mounting, if Humidity Indicator Card reads >10%

If baking is required, Devices may be baked for 8 hrs at 125 °C.

9.2. SMT Recommendation

- **Recommended Reflow profile：**



No.	Item	Temperature (°C)	Time (sec)
1	Pre-heat	D1: 140 ~ D2: 200	T1: 80 ~ 120
2	Soldering	D2: = 220	T2: 60 +/- 10
3	Peak-Temp.	D3: 250 °C max	

Note: (1) Reflow soldering is recommended two times maximum.
(2) Add Nitrogen while Reflow process： SMT solder ability will be better.

- **Stencil thickness**： 0.13~ 0.15 mm (Recommended)
- **Soldering paste (without Pb)**： Recommended SENJU N705-GRN3360-K2-V can get better soldering effects.

10. History Change

Revision	Date	Description
R 0.1	2009/05/26	New release
R 0.2	2009/07/13	Modify Storage/Operating Temperature Range, Pin out description & Reference Schematic
R 0.3	2009/08/10	Update Section 6 Reference Schematic, Section 7 Mechanical Figure for Pin1 indicator, Section 8.2 Recommended Stencil Design, Section 9 Baking Condition.